SHIVAJI UNIVERISTY, KOLHAPUR-416 004. MAHARASHTRA
PHONE : EPABX-2609000 **website- www.unishivaji.ac.in**
FAX 0091-0231-2691533 & 0091-0231-2692333 – BOS - 2609094
शिवाजी विद्यापीठ, कोल्हापूर – 416004.
दुरध्वनी (ईपीएबीएक्स) २६०९००० (अभ्यास मंडळे विभाग– २६०९०९४)
फॅक्स : ००९१-०२३१-२६९१५३३ व २६९२३३३.e-mail:bos@unishivaji.ac.in

" A" Re-accredited By NAAC (2014) with CGPA-3.16

SU/BOS/Engg./ 40 **Date: 15-06-2016**

The Principal/Director
of all Affiliated Engineering Colleges/Institutions/Departments
Shivaji University, Kolhapur.

Sub-: Regarding revised structure, syllabi & equivalance of the various branches under the Faculty of Engineering & Technology.

Sir/Madam,

With reference to the subject mentioned above, I am directed to inform you that the university authorities have accepted and granted approval to the revised structure, syllabi & equivalence of the following branches under the Faculty of Engineering & Technology.

1	**All Branches (except Electrical and Electronics, Architecture & Textile)**	**Structure & syllabi of B.E Part I & II (Semester VII & VIII)**
2	**M.Text (TT/TC/Tech/Text)**	**Structure & Syllabi of M.Text (TT/TC/Tech/Text)**
3	**Bachelor of Textile (B.Text.)**	**Structure & Syllabus of B.Text Sem Part II (Semester III & IV)**
4	**Bachelor of Technology**	**Structure & Syllabus of B.Tech. First Year (Sem. I & II)**
5	**Bachelor of Technology**	**Structure & syllabi of B.Tech. Final Year Mechanical Sem VII & VIII**
6	**M.Tech.**	**Structure & Syllabus of M.Tech. Envioronmental, Computer Science, Electronics, Food Technology & Energy Technology**
7	**Electrical & Electronics Engineering**	**Exetention has been given to existing Structure & Syllabi of B.E. Electrical & Electronics Engineering.**
8	**B.Architecture**	**Structure & Syllabi of First Year B.Architecture Sem. I & II (C.B.C.S.)**

The revised syllabi shall be implemented from the academic year 2016-17 (i.e. from July 2016) onwards. A CD containing revised structure, syllabi and equivalance is enclosed herewith. The revised syllabi is also made available on university website www.unishivaji.ac.in. Further, it is hereby informed that the question papers on the pre-revised syllabi shall be set for the examination to be held in October/November 2016 and April/May 2017. These chances are available for repeater students, if any.

You are therefore, requested to bring this to the notice of all students and techers concerned.

Thanking you,

Yours faithfully,

Sd/-

Dy. Registrar

Encl-: as above.
Copy to-
1)Co-Ordinater, Faculty of Engineering & Technology } **For information**
2) The Chairman, respective Co-ordination Commettee }
3) O.E. 4 Section
4) Affiliation Section
5) Appointment Sectionce
6) Eligibility Section **For information & necessary action .**
7) P.G. Admission Section
8) P.G.Seminar Section
9) Meeting Section
10) Computer Center

Estd. 1962
NAAC 'A' Grade,
MHRD NIRF- 28th Rank.

SHIVAJI UNIVERISTY, KOLHAPUR-416 004. MAHARASHTRA
PHONE : EPABX-2609000 **website- www.unishivaji.ac.in**
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दुरध्वनी (ईपीएबीएक्स) २६०९००० (अभ्यास मंडळे विभाग– २६०९०९४)
फॅक्स : ००९१-०२३१-२६९१५३३ व २६९२३३३.e-mail:bos@unishivaji.ac.in

SU/BOS/Engg./6097 Date: 05-10-2016

The Principal/Director,
of all Affiliated Engineering Colleges/Institutions/Departments,
Shivaji University, Kolhapur.

Sub:- Regarding new syllabus & structure of the M. E. Industrial Engg. (Sem I to IV) under the Faculty of Engineering & Technology.

Sir/Madam,

With reference to the subject mentioned above, I am directed to inform you that the University authorities have accepted and granted approval to new syllabus & structure of the M. E. Industrial Engg. (Sem I to IV) under the Faculty of Engg. & Technology.

The new syllabi shall be implemented from the academic year 2016-17 (i.e. from July 2016) onwards. A soft copy containing new structure, syllabus is enclosed herewith. The syllabus is also made available on University website www.unishivaji.ac.in.

You are therefore, requested to bring this to the notice of all students and teachers concerned.

Thanking you,

Yours faithfully,

Sd/-
Dy. Registrar

Encl:- as above.

Copy to-

1) The Co-ordinator, Faculty of Engg. & Technology
2) The Chairman, Co-ordinating committee in Production Engg.

} For information

3) O.E. 4 Section
4) Affiliation Section
5) Appointment Section
6) Eligibility Section
7) P.G. Admission Section
8) P.G.Seminar Section
9) ICT Cell

} For information & necessary action .

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES
Course Structure and Scheme of Evaluation
Semester I

Syllabus w.e.f from Academic year 2016-2017

Course Code	Course	Teaching Scheme			
		L	T	P	Credits
C 10	Research Methodology (Audit)	2	-	-	-
C11	High Speed Analog Design	4	-	-	4
C12	Reconfigurable Platforms & HDL	4	-	-	4
C 13	Communication Networks	4	-	-	4
E 14	Elective-I	3	-	-	3
E 15	Elective-II (open Elective*)	2	-	-	3
C 14	High Speed Analog Design Lab	-	-	2	1
C 15	Reconfigurable Platforms & HDL Lab	-	-	2	1
C 16	Communication Networks Lab	-	-	2	1
S 16	Seminar –I	-	-	2	2
	Total	20	0	8	23
Total contact hours per week= 28					

Elective - I

E14(V) Memory Technologies
E 14 (V) CMOS VLSI Design
E14(E) Asynchronous Circuit Design
E 14 (E) Advanced Computer Architecture

Elective - II

Choose from list on next page.

Elective - II
(Open Elective*)

Sr. No.	Elective – II (open Elective*)	Branch
1	E15(V) Digital System And Testing	Electronics Technology
2	E 15 (V)Mixed Signal ASIC Design	
3	E 15 (E) Automotive Embedded Systems	
4	FTE-21 : Advances in processing of dairy Technology	Food Technology
5	FTE-22 : food rheology and texture	
6	FTE-23: Advances in cereals and pulses processing technology.	
7	ETE2 Fuel and combustion Technology	Energy Technology
8	ETE2 solar passive architecture	
9	ETE2Energy storage systems	
10	ESTE-21 Optimization Techniques	Environmental Science and Technology
11	ESTE-22 Design of Energy efficient buildings	
12	ESTE-23 operational health and safety management	
13	CS515 Advanced Operating Systems	Computer Science and Technology
14	CS515 Real Time Systems	
15	CS515 Web Engineering	

Minimum Number of students for selection of Elective -8

Minimum Number of students for selection of Elective -36*

Preference will be given to core branch

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES
Course Structure and Scheme of Evaluation
Semester II

Syllabus w.e.f from Academic year 2016-2017

Course Code	Course	Teaching Scheme			
		L	T	P	Credits
C 21	DSP Processor	4	-	-	4
C22	Real Time Operating System	4	-	-	4
C23	Mobile Computing	4	-	-	4
E 24	Elective-III	3	-	-	3
E 25	Elective- IV	3	-	-	3
C 24	DSP Processor Lab	-	-	2	1
C 25	Real Time Operating System Lab	-	-	2	1
C 26	Mobile Computing Lab	-	-	2	1
C 29	Seminar –II	-	-	2	1
	Total	18	0	8	23
Total contact hours per week= 26					

Elective - III

E24(V) System on Chip
E 24 (V) Wavelet Transform and Applications
E24(E) Micro Elctro Mechanical System
E 24 (E) Robotics and Machine Vision

Elective - IV

Choose from list on next page.

Elective - IV
(Open Elective*)

Sr. No.	Elective – IV (open Elective*)	Branch
1	E25(V) RF Integrated Circuit Design	Electronics Technology
2	E25(E) High Performance Networks	
3	E25(E) High Speed Digital Design	
4	FTE-41 : Recent developments in processing of plantation crops	Food Technology
5	FTE-42 : Simulation and modeling in food processing	
6	FTE-43: project management for food processing industries.	
7	ETE 4-1 Power co-generation	Energy Technology
8	ETE 4-2 Energy modeling and project management	
9	ETE 4-3 The new Energy technologies	
10	ESTE-41 Operation and maintenance of environmental facilities	Environmental Science and Technology
11	ESTE-42 Rural water supply and sanitation	
12	ESTE-43 Environmental Technology	
13	CS525 Geographical Information Systems	Computer Science and Technology
14	CS525 Artificial Intelligence and Natural Language Processing	
15	CS525 System modeling and simulation	

Minimum Number of students for selection of Elective - 8

Minimum Number of students for selection of Elective - 36*

Preference will be given to core branch

SHIVAJI UNIVERSITY
M.TECH (Electronics Technology) PROGRAMMES
Semester III

Course code	course	Teaching scheme			
		L	T	P	credit
T 31	Industrial Training	-	-	**2	4
S 32	Dissertation phase-1	-	-	**5	10
	Total	-	-	7	14
	**Total contact hours per week/students = 2 & 5 respectively for T31 & S 32				

***8 weeks at the end of first year**

OR

Industrial training will be split in two slots of four weeks during semester III

Semester IV

Course code	course	Teaching scheme			
		L	T	P	credit
D 42	Dissertation phase-2	-	-	5	20
	Total	-	-	5	20
	**Total contact hours per week = 5				

Shivaji University, Kolhapur First Year M. Tech Electronics Technology (Semester I)	
1. C-10 Research Methodology (Audit)	**Research Methodology (Audit)**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 2 hrs/week T: -- Credits: --	Teaching Scheme : L : 2 hrs/week T: -- Credits: --
Unit 1 **4 HRS** **Research Methodology: An Introduction** Objectives of Research, Types of Research, Research Methods and Methodology, Defining a Research Problem, Techniques involved in Defining a Problem	**Unit 1** **4 HRS** **Research Methodology: An Introduction** Objectives of Research, Types of Research, Research Methods and Methodology, Defining a Research Problem, Techniques involved in Defining a Problem
Unit 2 **6 HRS** **Research Design** Need for Research Design, Features of Good Design, Different Research Designs, Basic Principles of Experimental Designs, Sampling Design, Steps In Sampling Design, Types of Sampling Design, Sampling Fundamentals, Estimation, Sample size Determination, Random sampling	**Unit 2** **6 HRS** **Research Design** Need for Research Design, Features of Good Design, Different Research Designs, Basic Principles of Experimental Designs, Sampling Design, Steps In Sampling Design, Types of Sampling Design, Sampling Fundamentals, Estimation, Sample size Determination, Random sampling
Unit 3 **4 HRS** **Measurement and Scaling Techniques** Measurement in Research, Measurement Scales, Scales, Sources in Error, Techniques of Developing Measurement Tools, Scaling, Meaning of Scale, Scale Construction Techniques.	**Unit 3** **4 HRS** **Measurement and Scaling Techniques** Measurement in Research, Measurement Scales, Scales, Sources in Error, Techniques of Developing Measurement Tools, Scaling, Meaning of Scale, Scale Construction Techniques.
Unit 4 **4 HRS** **Methods of Data Collection and Analysis** Collection of Primary and Secondary Data, Selection of appropriate method, Data Processing Operations, Elements of Analysis, Statistics in Research, Measures of Dispersion, Measures of Skewness, Regression Analysis, Correlation	**Unit 4** **4 HRS** **Methods of Data Collection and Analysis** Collection of Primary and Secondary Data, Selection of appropriate method, Data Processing Operations, Elements of Analysis, Statistics in Research, Measures of Dispersion, Measures of Skewness, Regression Analysis, Correlation
Unit 5 **4 HRS** **Techniques of Hypotheses, Parametric or Standard Tests** Basic concepts, Tests for Hypotheses I and II, Important parameters, Limitations of the tests of Hypotheses, Chi-square Test, Comparing Variance, as a non-parametric Test, Conversion of Chi to Phi, Caution in Using Chi- square test	**Unit 5** **4 HRS** **Techniques of Hypotheses, Parametric or Standard Tests** Basic concepts, Tests for Hypotheses I and II, Important parameters, Limitations of the tests of Hypotheses, Chi-square Test, Comparing Variance, as a non-parametric Test, Conversion of Chi to Phi, Caution in Using Chi- square test
Unit 6 **4 HRS** **Analysis of Variance and Co-variance** ANOVA, One way ANOVA, Two Way ANOVA, ANOCOVA, Assumptions in ANOCOVA, Multivariate Analysis Technique, Classification of Multivariate Analysis, factor Analysis, R-type Q Type Factor Analysis, Path Analysis	**Unit 6** **4 HRS** **Analysis of Variance and Co-variance** ANOVA, One way ANOVA, Two Way ANOVA, ANOCOVA, Assumptions in ANOCOVA, Multivariate Analysis Technique, Classification of Multivariate Analysis, factor Analysis, R-type Q Type Factor Analysis, Path Analysis
Unit 7 Interpretation and Report **1**	**Interpretation and Report** **1**

2. C-11 High Speed Analog Design Techniques	**High Speed Analog Design Techniques**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 4 hrs/week Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 4 hrs/week Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 High Speed Operational Amplifiers 6 HRS Folded Cascode Voltage Feedback Op-Amps, Case study of AD847, Current Feedback Op-Amps (CFB), CFB model and Bode plot, study of AD8011, Comparison of specifications of Current feedback Op-amp family AD8001, AD8002, AD8009 and AD8073, Noise comparisons between VFB and CFB Op Amps, PSRR Characteristics.	**Unit 1 High Speed Operational Amplifiers 6 HRS** Folded Cascode Voltage Feedback Op-Amps, Case study of AD847, Current Feedback Op-Amps (CFB), CFB model and Bode plot, study of AD8011, Comparison of specifications of Current feedback Op-amp family AD8001, AD8002, AD8009 and AD8073, Noise comparisons between VFB and CFB Op Amps, PSRR Characteristics.
Unit 2 High-Speed applications based on Op-amps 7 HRS Optimizing feedback network for maximum bandwidth fitness, Driving Capacitive load, Cable drivers and receivers, High performance video line driver, Differential line drivers and receivers, High speed clamping amplifiers, High speed current to voltage converters and the effects of inverting input capacitance	**Unit 2 High-Speed applications based on Op-amps 7 HRS** Optimizing feedback network for maximum bandwidth fitness, Driving Capacitive load, Cable drivers and receivers, High performance video line driver, Differential line drivers and receivers, High speed clamping amplifiers, High speed current to voltage converters and the effects of inverting input capacitance
Unit 3 6 HRS High speed amplifiers for communication applications Low noise amplifiers for communication systems, Mixers, Power amplifiers, Liner drivers, Automatic gain control amplifiers	**Unit 3 6 HRS** High speed amplifiers for communication applications Low noise amplifiers for communication systems, Mixers, Power amplifiers, Liner drivers, Automatic gain control amplifiers
Unit 4 7 HRS High speed video multiplexing with Opamps using disable function, Video programmable gain amplifier, Video multiplexers and Cross Point switches, High power line drivers and ADSL, High speed photodiode Pre amps, Case studies of AD830, AD9002	**Unit 4 7 HRS** High speed video multiplexing with Opamps using disable function, Video programmable gain amplifier, Video multiplexers and Cross Point switches, High power line drivers and ADSL, High speed photodiode Pre amps, Case studies of AD830, AD9002
Unit 5 6 HRS Dynamic range compression, Linear VCAs, Log/Limiting Amplifiers, Receiver overview, Multipliers, modulators and mixers,	**Unit 5 6 HRS** Dynamic range compression, Linear VCAs, Log/Limiting Amplifiers, Receiver overview, Multipliers, modulators and mixers,
Unit 6 7 HRS Case study of AD600 Dual Channel X-amp, AD641 monolithic log amplifier.	**Unit 6 7 HRS** Case study of AD600 Dual Channel X-amp, AD641 monolithic log amplifier.
References: 1. Intuitive Operational Amplifiers, Thomas M. Frederiksen, McGraw Hill, 1988. 2. B Razavi, "RF Microelectronics", Prentice Hall, 1998 3. T.H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits" Cambridge University Press, 1998. 4. High Speed Design Techniques, Manual by analog Devices, October 1996	**References:** 1. Intuitive Operational Amplifiers, Thomas M. Frederiksen, McGraw Hill, 1988. 2. B Razavi, "RF Microelectronics", Prentice Hall, 1998 3. T.H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits" Cambridge University Press, 1998. 4. High Speed Design Techniques, Manual by analog Devices, October 1996

5. Modular Low-Power, High Speed CMOS Analog-to-Digital Converter for Embedded Systems, Lin, Dr. Ing.Keh-La Kemma, Armin Hosticka, Prof. Bedrich J. Publisher, Kluwer Academic Publishers	5. Modular Low-Power, High Speed CMOS Analog-to-Digital Converter for Embedded Systems, Lin, Dr. Ing.Keh-La Kemma, Armin Hosticka, Prof. Bedrich J. Publisher, Kluwer Academic Publishers

3. C 12 Reconfigurable Platforms and HDL	**C 12 Reconfigurable Platforms and HDL**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 4 hrs/week Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 4 hrs/week Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Computing requirements, Area, Technology scaling, Instructions,Custom ComputingMachine, Overview, Comparison of Computing Machines.	**Unit 1** **6 HRS** Computing requirements, Area, Technology scaling, Instructions,Custom ComputingMachine, Overview, Comparison of Computing Machines.
Unit 2 **7 HRS** Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUT's, LUT Mapping, ALU and CLB's, Retiming, Fine-grained & Coarse-grained structures; Multicontext; Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories.	**Unit 2** **7 HRS** Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUT's, LUT Mapping, ALU and CLB's, Retiming, Fine-grained & Coarse-grained structures; Multicontext; Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories.
Unit 3 **6 HRS** Arrays for fast computations, CPLDs, FPGAs, Multicontext, Partial Reconfigurable Devices; TSFPGA, DPGA, Mattrix; Best suitable approach for RD; Case study. Control Logic, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Best suitable methods for RD.	**Unit 3** **6 HRS** Arrays for fast computations, CPLDs, FPGAs, Multicontext, Partial Reconfigurable Devices; TSFPGA, DPGA, Mattrix; Best suitable approach for RD; Case study. Control Logic, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Best suitable methods for RD.
Unit 4 **7 HRS** Contexts, Context switching; Area calculations for PE;Efficiency, ISP, Hot Reconfiguration; Case study. Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research.	**Unit 4** **7 HRS** Contexts, Context switching; Area calculations for PE;Efficiency, ISP, Hot Reconfiguration; Case study. Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research.
Unit 5 **6 HRS** Software challenges in System on chip; Testability challenges; Case studies. Modeling, Temporal portioning algorithms, Online	**Unit 5** **6 HRS** Software challenges in System on chip; Testability challenges; Case studies. Modeling, Temporal portioning algorithms, Online temporal

temporal placement, Device space management.	placement, Device space management.
Unit 6 **7 HRS** Direct communication, Third party communication, Bus based communication, Circuit switching, Network on chip, Dynamic network on chip, Partial reconfigurable design.	**Unit 6** **7 HRS** Direct communication, Third party communication, Bus based communication, Circuit switching, Network on chip, Dynamic network on chip, Partial reconfigurable design.
References- 1. Andre Dehon, "Reconfigurable Architectures for General Purpose Computing". 2. IEEE Journal papers on Reconfigurable Architectures. 3. "High Performance Computing Architectures" (HPCA) Society papers. 4. Christophe Bobda, "Introduction to Reconfigurable Computing", Springer Publication. 5. Maya Gokhale, Paul Ghaham, "Reconfigurable Computing", Springer Publication.	**References-** 1. Andre Dehon, "Reconfigurable Architectures for General Purpose Computing". 2. IEEE Journal papers on Reconfigurable Architectures. 3. "High Performance Computing Architectures" (HPCA) Society papers. 4. Christophe Bobda, "Introduction to Reconfigurable Computing", Springer Publication. 5. Maya Gokhale, Paul Ghaham, "Reconfigurable Computing", Springer Publication.

4. C 13 Communication Networks	**Communication Networks**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 4 hrs/week T : -- Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 4 hrs/week T : -- Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Advanced IPv6 features, including transition. Mobile IPv6 operation. Models to support (WLAN) network roaming , IPv6 transition methods ;	**Unit 1** **6 HRS** TCP/IP fundamentals, Reviews on wireless communication technologies, WLAN, Bluetooth, TCP/IP over Wireless Networks
Unit 2 **7 HRS** Advanced IP routing and multihoming, Challenging networking scenarios. Advanced security issues ' Network performance and monitoring. Advanced IP Multicast	**Unit 2** **7 HRS** Advanced IP routing and multihoming, Challenging networking scenarios. Advanced security issues ' Network performance and monitoring. Advanced IP Multicast
Unit 3 **6 HRS** Link-local and Adminstrator-less networking.Topics in Dynamic Host Configuration, Node and Service Discovery, Multi-homing in Enterprise networks. Issues with renumbering live networks	**Unit 3** **6 HRS** Link-local and Adminstrator-less networking.Topics in Dynamic Host Configuration, Node and Service Discovery, Multi-homing in Enterprise networks. Issues with renumbering live networks
Unit 4 **7 HRS** TCP/IP fundamentals, Reviews on wireless communication technologies, WLAN, Bluetooth, TCP/IP over Wireless Networks	**Unit 4** **7 HRS** Advanced IPv6 features, including transition. Mobile IPv6 operation. Models to support (WLAN) network roaming , IPv6 transition methods ;
Unit 5 **6 HRS** Routing, Multicast, Content Distribution Networks, Content addressing, search, and retrieval	**Unit 5** **6 HRS** Routing, Multicast, Content Distribution Networks and retrieval

Unit 6 **7 HRS** Bluetooth, 802.11. HiperLAN2, GPRS and Edge Services, UMTS, 3G, Beyond 3G: integrated 4G services. Access technologies: last mile, xDSL, Reviews of packet switching, Advanced topics in Computer Networking Multimedia over a Network, Streaming over Internet, Streaming over wired and wireless Network, Wireless Sensor Networks, Wireless Home Networks	**Unit 6** **7 HRS** Bluetooth, 802.11. HiperLAN2, GPRS and Edge Services, UMTS, 3G, Beyond 3G: integrated 4G services. Access technologies: last mile, xDSL, Reviews of packet switching, Advanced topics in Computer Networking Multimedia over a Network, Streaming over Internet, Streaming over wired and wireless Network, Wireless Sensor Networks, Wireless Home Networks
References: 1. Computer Networking: A Top-Down Approach Featuring the Internet, by James Kwose and Keith Ross, ISBN: 0-201-97699-4, Addison-Wesley, 2/e, 2002 2. IP SANS: A Guide to iSCSI, iFCP, and FCIP Protocols for Storage Area Networks, by Thomas dark, ISBN: 0-201-75277-8, Addison-Wesley, 2002 3. Storage Area Network Fundamentals, by Meeta Gupta, ISBN: I-58705-065-X, Prentice Hall, April 2002 4. Designing Storage Area Networks: A Practical Reference for Implementing Fibre Channel and IP SANs, 2/E, by Tom dark, ISBN: 0-321-13650-0, Addison-Wesley, 2003 5. Wireless Communications and Networks, by William Stallings, ISBN: 0-13-040864-6, Prentice Hall, 2002 6. Computer Networks: A Systems Approach, 2/e, by Lan-y Peterson and Bruce Davie, ISBN: 1-55860-514-2, Morgan Kaufinann Publishers, 2000	**References:** 1. Computer Networking: A Top-Down Approach Featuring the Internet, by James Kwose and Keith Ross, ISBN: 0-201-97699-4, Addison-Wesley, 2/e, 2002 2. IP SANS: A Guide to iSCSI, iFCP, and FCIP Protocols for Storage Area Networks, by Thomas dark, ISBN: 0-201-75277-8, Addison-Wesley, 2002 3. Storage Area Network Fundamentals, by Meeta Gupta, ISBN: I-58705-065-X, Prentice Hall, April 2002 4. Designing Storage Area Networks: A Practical Reference for Implementing Fibre Channel and IP SANs, 2/E, by Tom dark, ISBN: 0-321-13650-0, Addison-Wesley, 2003 5. Wireless Communications and Networks, by William Stallings, ISBN: 0-13-040864-6, Prentice Hall, 2002 6. Computer Networks: A Systems Approach, 2/e, by Lan-y Peterson and Bruce Davie, ISBN: 1-55860-514-2, Morgan Kaufinann Publishers, 2000

5. ELECTIVE-I E14 (V) Memory Technologies	**ELECTIVE-I E14 (V) Memory Technologies**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs;	**Unit 1** **6 HRS** Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs;
Unit 2 **7 HRS** DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM,	**Unit 2** **7 HRS** DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM,

Advanced DRAM Design and Architecture, Application Specific DRAM,	Advanced DRAM Design and Architecture, Application Specific DRAM,
Unit 3 **6 HRS** High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory	**Unit 3** **6 HRS** High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory
Unit 4 **7 HRS** Testing.General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP,Radiation Hardening Techniques.	**Unit 4** **7 HRS** Testing.General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP,Radiation Hardening Techniques.
Unit 5 **6 HRS** Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.	**Unit 5** **6 HRS** Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.
Unit 6 **7 HRS** Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.	**Unit 6** **7 HRS** Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.
References- 1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997. 2. Memories", Springer Publication. 3. Wen C. Lin, "Handbook of Digital System Design", CRC Press.	**References-** 1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997. 2. Memories", Springer Publication. 3. Wen C. Lin, "Handbook of Digital System Design", CRC Press.

5. Elective – I E14 (V) CMOS VLSI Design	**Elective – I E14 (V) CMOS VLSI Design**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** VLSI Design: History, Trends, Principles, Metrics, CMOS transistors (n-channel andp-channel), The CMOS Switch model, CMOS Inverter mode, Logic devices and interconnect, CMOS circuit analysis: transistors, inverters, interconnect modeling, parasitics, CMOS Process and Layout, CMOS Devices: SPICE and deep sub-micron issues	**Unit 1** **6 HRS** VLSI Design: History, Trends, Principles, Metrics, CMOS transistors (n-channel andp-channel), The CMOS Switch model, CMOS Inverter mode, Logic devices and interconnect, CMOS circuit analysis: transistors, inverters, interconnect modeling, parasitics, CMOS Process and Layout, CMOS Devices: SPICE and deep sub-micron issues

Unit 2 **7 HRS** CMOS Inverter: speed, power and scaling, Static CMOS Gates, Dynamic CMOS Gates, Power Estimation and Optimization	**Unit 2** **7 HRS** CMOS Inverter: speed, power and scaling, Static CMOS Gates, Dynamic CMOS Gates, Power Estimation and Optimization
Unit 3 **6 HRS** Analytical modeling: Ellmore Delay, Transmission models, RC, RLC lumped parameter models, Layout for custom logic: Sea of Gates (SoG) model, Design rules, Circuit fabrication methods for CMOS, Levels of abstraction.	**Unit 3** **6 HRS** Analytical modeling: Ellmore Delay, Transmission models, RC, RLC lumped parameter models, Layout for custom logic: Sea of Gates (SoG) model, Design rules, Circuit fabrication methods for CMOS, Levels of abstraction.
Unit 4 **7 HRS** VLSI circuits to systems, Circuit modeling and layout (demo using standard tools), CMOS design and layout tools, Nano-electronics circuits versus CMOS microelectronics circuits, Nano-computing techniques and device platforms	**Unit 4** **7 HRS** VLSI circuits to systems, Circuit modeling and layout (demo using standard tools), CMOS design and layout tools, Nano-electronics circuits versus CMOS microelectronics circuits, Nano-computing techniques and device platforms
Unit 5 **6 HRS** Digital CMOS IC design: Sequential Logic Circuits, Implementation Strategies for Digital ICs, Interconnects, Timing and Clocking, Datapath Design, Memory Design, Capactitiveparasitics, Resistive parasitics, Inductive parasitics	**Unit 5** **6 HRS** Digital CMOS IC design: Sequential Logic Circuits, Implementation Strategies for Digital ICs, Interconnects, Timing and Clocking, Datapath Design, Memory Design, Capactitiveparasitics, Resistive parasitics, Inductive parasitics
Unit 6 **7 HRS** Timing Issues, Clock skew, clocking styles, Self-timed circuit design, Case study of Kitchen timer chip	**Unit 6** **7 HRS** Timing Issues, Clock skew, clocking styles, Self-timed circuit design, Case study of Kitchen timer chip
References- 1. N.H.E. Weste and K. Eshraghian, “Principles of CMOS VLSI Design”, New Uork: Addison-Wesley, 1993. 2. Christopher Saint and Judy Saint, “IC Layout Basics”, McGraw Hill Publications 3. Weste and Harris, CMOS VLSI Design, a Circuits and Systems Perspective (3 rd edition) 4. by Jan M. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits (2nd Edition) Prentice Hall, 2003.	**References-** 1. N.H.E. Weste and K. Eshraghian, “Principles of CMOS VLSI Design”, New Uork: Addison-Wesley, 1993. 2. Christopher Saint and Judy Saint, “IC Layout Basics”, McGraw Hill Publications 3. Weste and Harris, CMOS VLSI Design, a Circuits and Systems Perspective (3 rd edition) 4. by Jan M. Rabaey, A. Chandrakasan, B. Nikolic, Digital Integrated Circuits (2nd Edition) Prentice Hall, 2003.

5. Elective – I - E 14 (E) Asynchronous Circuit Design			**Asynchronous Circuit Design**		
Old Syllabus			**New Syllabus**		
Teaching Scheme : L : 3hrs/week		Credits: 3	Teaching Scheme : L : 3hrs/week		Credits: 3
Evaluation Scheme: CIE (25 + 25)	SEE 50	Minimum Passing Marks 40	Evaluation Scheme: CIE (25 + 25)	SEE 50	Minimum Passing Marks 40
Unit 1 **6 HRS**			**Unit 1** **6 HRS**		

Introduction to asynchronous circuit design, Communication channels, Modeling asychronous communication in VHDL,Example: MiniMIPS	Introduction to asynchronous circuit design, Communication channels, Modeling asychronous communication in VHDL,Example: MiniMIPS
Unit 2 **7 HRS** Communication protocols, Handshaking expansion, Data Encoding, Syntax-directed translation,Graphical representations, Asynchronous finite state machines, Petri nets,Timed event/level structures	**Unit 2** **7 HRS** Communication protocols, Handshaking expansion, Data Encoding, Syntax-directed translation,Graphical representations, Asynchronous finite state machines, Petri nets,Timed event/level structures
Unit 3 **6 HRS** Huffman circuits, Solving covering problems, State minimization, State assignment,Hazard-free logic synthesis, Extensions for MIC operation	**Unit 3** **6 HRS** Huffman circuits, Solving covering problems, State minimization, State assignment,Hazard-free logic synthesis, Extensions for MIC operation
Unit 4 **7 HRS** Muller circuits, Complete state coding Hazard-free logic synthesis, Hazard-free ,decomposition	**Unit 4** **7 HRS** Muller circuits, Complete state coding Hazard-free logic synthesis, Hazard-free ,decomposition
Unit 5 **6 HRS** Timing circuits, Zones, POSET Timing,Verification , Circuit verification ,Protocal verification	**Unit 5** **6 HRS** Timing circuits, Zones, POSET Timing,Verification , Circuit verification ,Protocal verification
Unit 6 **7 HRS** Applications , History/RAPPID , Performance analysis/testing , Synchronization problem	**Unit 6** **7 HRS** Applications , History/RAPPID , Performance analysis/testing , Synchronization problem
References- "Asynchronous Circuit Design", Chris J. Myers, John Wiley & Sons, Inc	References- "Asynchronous Circuit Design", Chris J. Myers, John Wiley & Sons, Inc

5. Elective – I E 14 (E) Advanced Computer Architecture	**Advanced Computer Architecture**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** ILP – Concepts and challenges – Hardware and software approaches – Dynamic scheduling – Speculation - Compiler techniques for exposing ILP – Branch prediction.	**Unit 1** **6 HRS** ILP – Concepts and challenges – Hardware and software approaches – Dynamic scheduling – Speculation - Compiler techniques for exposing ILP – Branch prediction.

Unit 2 **7 HRS** VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism – Hardware versus software speculation mechanisms – IA 64 and Itanium processors – Limits on ILP.	**Unit 2** **7 HRS** VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism – Hardware versus software speculation mechanisms – IA 64 and Itanium processors – Limits on ILP.
Unit 3 **6 HRS** Symmetric and distributed shared memory architectures – Performance issues – Synchronization – Models of memory consistency – Introduction to Multithreading.	**Unit 3** **6 HRS** Symmetric and distributed shared memory architectures – Performance issues – Synchronization – Models of memory consistency – Introduction to Multithreading.
Unit 4 **7 HRS** Cache performance – Reducing cache miss penalty and miss rate – Reducing hit time – Main memory and performance – Memory technology. Types of storage devices – Buses – RAID – Reliability, availability and dependability – I/O performance measures – Designing an I/O system.	**Unit 4** **7 HRS** Cache performance – Reducing cache miss penalty and miss rate – Reducing hit time – Main memory and performance – Memory technology. Types of storage devices – Buses – RAID – Reliability, availability and dependability – I/O performance measures – Designing an I/O system.
Unit 5 **6 HRS** Software and hardware multithreading – SMT and CMP architectures – Design issues –	**Unit 5** **6 HRS** Software and hardware multithreading – SMT and CMP architectures – Design issues –
Unit 6 **7 HRS** Case studies – Intel Multi-core architecture – SUN CMP architecture - heterogenous multi-core **7hrs.** processors – case study: IBM Cell Processor.	**Unit 6** **7 HRS** Case studies – Intel Multi-core architecture – SUN CMP architecture - heterogenous multi-core **7hrs.** processors – case study: IBM Cell Processor.
TEXT BOOKS: 1. John L. Hennessey and David A. Patterson, " Computer architecture – A quantitative approach", Morgan Kaufmann / Elsevier Publishers, 4th. edition, 2007**.** REFERENCES: 1. David E. Culler, Jaswinder Pal Singh, "Parallel computing architecture: A hardware/software approach" , Morgan Kaufmann /Elsevier Publishers, 1999. 2. Kai Hwang and Zhi.WeiXu, "Scalable Parallel Computing", Tata McGraw Hill, New Delhi, 2003.	TEXT BOOKS: 1. John L. Hennessey and David A. Patterson, " Computer architecture – A quantitative approach", Morgan Kaufmann / Elsevier Publishers, 4th. edition, 2007**.** REFERENCES: 1. David E. Culler, Jaswinder Pal Singh, "Parallel computing architecture: A hardware/software approach" , Morgan Kaufmann /Elsevier Publishers, 1999. 2. Kai Hwang and Zhi.WeiXu, "Scalable Parallel Computing", Tata McGraw Hill, New Delhi, 2003.

6. Elective – II E 15 (V) Digital Systems and Testing	Digital Systems and Testing
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Testing Defined: definitions and areas within testing. Logic and Fault Modeling.Mechanics Definitions: Abstractions level, Faults and errors , Modeling, Test Evaluation, Test Generation, Diagnostics.	**Unit 1** **6 HRS** Testing Defined: definitions and areas within testing. Logic and Fault Modeling.Mechanics Definitions: Abstractions level, Faults and errors , Modeling, Test Evaluation, Test Generation, Diagnostics.
Unit 2 **7 HRS** Representation and models of digital systems across abstraction levels.Fault Models: logical versus physical; SSL model, opens and shorts, bridging faults; Basic assumptions.Review of minimization tools and asynchronous machines, Test Pattern Generation basics. (activate and drive.), Algebraic approaches, Fault Equivalence and Dominance.	**Unit 2** **7 HRS** Representation and models of digital systems across abstraction levels.Fault Models: logical versus physical; SSL model, opens and shorts, bridging faults; Basic assumptions.Review of minimization tools and asynchronous machines, Test Pattern Generation basics. (activate and drive.), Algebraic approaches, Fault Equivalence and Dominance.
Unit 3 **6 HRS** Algebraic Approaches and Structural Approaches, Logic Simulation. Algebraic Approaches: Boolean difference, Literal position, Effect of fanout on circuits, Checkpoint faults. Structural Approaches to test generation. Path sensitization methods. Test Coverage	**Unit 3** **6 HRS** Algebraic Approaches and Structural Approaches, Logic Simulation. Algebraic Approaches: Boolean difference, Literal position, Effect of fanout on circuits, Checkpoint faults. Structural Approaches to test generation. Path sensitization methods. Test Coverage
Unit 4 **7 HRS** Simulation engines: compiler, event driven. Representation of value, circuit, etc. Logic and Fault Simulation: Delay models for circuit simulation, Fault Simulation Purpose of Serial and Parallel Fault Simulation, Deductive fault simulation. Concurrent Fault Simulation, Critical Path tracing, Statistical Fault Analysis	**Unit 4** **7 HRS** Simulation engines: compiler, event driven. Representation of value, circuit, etc. Logic and Fault Simulation: Delay models for circuit simulation, Fault Simulation Purpose of Serial and Parallel Fault Simulation, Deductive fault simulation. Concurrent Fault Simulation, Critical Path tracing, Statistical Fault Analysis
Unit 5 **7 HRS**	**Unit 5** **7 HRS**

D-algorithm.representation, cube algebra, generalized algorithm, Extensions to D-algorithm PODEM, FAN, etc. Random test generation, Complexity issues Functional Test Generation Methods, Heuristic Methods, Exhaustive and Pseudo Exhaustive techniques, RAM and PLA testing, Microprocessor testing, Memory Testing: Memory test complexity, Memory fault models.	D-algorithm.representation, cube algebra, generalized algorithm, Extensions to D-algorithm PODEM, FAN, etc. Random test generation, Complexity issues Functional Test Generation Methods, Heuristic Methods, Exhaustive and Pseudo Exhaustive techniques, RAM and PLA testing, Microprocessor testing, Memory Testing: Memory test complexity, Memory fault models.
Unit 6 **7 HRS** Controllability and Observabilitymeasures.STEFAN, Ad Hoc techniques, More Design for Testability, Scan Design.Scan Designs: IEEE Standards, Board-Level Testing: Boundary Scan, Data Compression and BIST, LFSR polynomial generation Data compression techniquesAliasing Probability, BIST, Self Checking and PLD Testing	**Unit 6** **7 HRS** Controllability and Observabilitymeasures.STEFAN, Ad Hoc techniques, More Design for Testability, Scan Design.Scan Designs: IEEE Standards, Board-Level Testing: Boundary Scan, Data Compression and BIST, LFSR polynomial generation Data compression techniquesAliasing Probability, BIST, Self Checking and PLD Testing
References: 1. "Digital Systems Testing and Testable Design" by MironAbramo Melvin Breuer and Arthur Friedman, IEEE press, NY. 2. A Guide to VHDL'' by Stanley Mazor, Kluwer Academic Press 3. "HDL Chip Design" by Douglas Smith, Doone Publications, AL. 4. "Rapid Prototyping of Digital Systems", by J. O. Hamblen and Furman, Kluwer Academic Publishers.	**References:** 1. "Digital Systems Testing and Testable Design" by MironAbramo Melvin Breuer and Arthur Friedman, IEEE press, NY. 2. A Guide to VHDL'' by Stanley Mazor, Kluwer Academic Press 3. "HDL Chip Design" by Douglas Smith, Doone Publications, AL. 4. "Rapid Prototyping of Digital Systems", by J. O. Hamblen and Furman, Kluwer Academic Publishers.

6. Elective – II E 15 (V) Mixed Signal ASIC Design	**Mixed Signal ASIC Design**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Technology and modeling aspects of an advanced BiCMOS ASIC process,LSI Logic analogue BiMOS technology, Background, Process technology, Well formation, Island definition and field region implants, Field oxidation - Island formation, High performance operational amplifiers and comparators High performance amplifiers, The load compensated OTA (LC-OTA), The Miller compensated OTA (M-OTA), The core-amplifier (C-OTA), High performance comparators, The OTA as comparator, Latched comparators, A high speed accurate comparator.	**Unit 1** **6 HRS** Technology and modeling aspects of an advanced BiCMOS ASIC process,LSI Logic analogue BiMOS technology, Background, Process technology, Well formation, Island definition and field region implants, Field oxidation - Island formation, High performance operational amplifiers and comparators High performance amplifiers, The load compensated OTA (LC-OTA), The Miller compensated OTA (M-OTA), The core-amplifier (C-OTA), High performance comparators, The OTA as comparator, Latched comparators, A high speed accurate comparator.
Unit 2 **7 HRS**	**Unit 2** **7 HRS**

Switched current techniques for analogue sampled data signal processing Introduction, First generation memory cells, Second generation memory cells, Limitations of the basic SI memory cell, Channel length modulation, Charge injection, Junction leakage Applications: Integrator based biquad, FIR filters, Sigma-Delta modulators	Switched current techniques for analogue sampled data signal processing Introduction, First generation memory cells, Second generation memory cells, Limitations of the basic SI memory cell, Channel length modulation, Charge injection, Junction leakage Applications: Integrator based biquad, FIR filters, Sigma-Delta modulators
Unit 3 **6 HRS** Parameters for data converter characterisation, Data converters: Basic design considerations, High speed data conversion techniques, Current switched D/A converters, Flash and two-step flash converters, Limits to speed and resolution in data converters Oversampling converters, Intuitive Introduction to Oversampling Data Converters, Noise shaping converters, First order sigma delta modulators Second order sigma delta modulator, Multistage sigma-delta modulator, Non ideal effects in sigma delta modulators, Sampling jitter	**Unit 3** **6 HRS** Parameters for data converter characterisation, Data converters: Basic design considerations, High speed data conversion techniques, Current switched D/A converters, Flash and two-step flash converters, Limits to speed and resolution in data converters Oversampling converters, Intuitive Introduction to Oversampling Data Converters, Noise shaping converters, First order sigma delta modulators Second order sigma delta modulator, Multistage sigma-delta modulator, Non ideal effects in sigma delta modulators, Sampling jitter
Unit 4 **7 HRS** Self-calibrated analogue-digital converters, Architecture with segmented binary-weighted capacitor Array, Self-calibration technique and circuits, Principle of calibration, Calibrating capacitors, Calibrating registers	**Unit 4** **7 HRS** Self-calibrated analogue-digital converters, Architecture with segmented binary-weighted capacitor Array, Self-calibration technique and circuits, Principle of calibration, Calibrating capacitors, Calibrating registers
Unit 5 **6 HRS** A high flexibility BiCMOS standard cell library for mixed analogue-digital ASICs A BiCMOS process dedicated to mixed A/D applications, Cell libraries, Analogue libraries, The digital cell library, CAD tools, The CAD capability, Telescopic Cells, Parametrizable cells, Adjustable cells, Automatic cell biasing and power down, ADS (Analog Design System) An environment for Mixed signal design, Analogue/digital multi-level mixed mode simulations, Case Studies: Example 1: Infra red receiver with decoder and actuator Example 2: Remote control	**Unit 5** **6 HRS** A high flexibility BiCMOS standard cell library for mixed analogue-digital ASICs A BiCMOS process dedicated to mixed A/D applications, Cell libraries, Analogue libraries, The digital cell library, CAD tools, The CAD capability, Telescopic Cells, Parametrizable cells, Adjustable cells, Automatic cell biasing and power down, ADS (Analog Design System) An environment for Mixed signal design, Analogue/digital multi-level mixed mode simulations, Case Studies: Example 1: Infra red receiver with decoder and actuator Example 2: Remote control
Unit 6 **7 HRS** Element matching, Local process variations, Global process variations, Process gradients, Boundary effects, Noise coupling,	**Unit 6** **7 HRS** Element matching, Local process variations, Global process variations, Process gradients, Boundary effects, Noise coupling,

Substrate noise coupling, Signal noise coupling, Examples of optimized structures, Few applications of mixed signal ASICs: Applications areas: A heart rate meter, Hearing aid ASIC, Sound and rhythm generator, TV picture in picture processor, A multi-standard modem, A speech scrambler de-scrambler.	Substrate noise coupling, Signal noise coupling, Examples of optimized structures, Few applications of mixed signal ASICs: Applications areas: A heart rate meter, Hearing aid ASIC, Sound and rhythm generator, TV picture in picture processor, A multi-standard modem, A speech scrambler de-scrambler.
References- 1. 1. Analogue-digital ASICs: circuit techniques, design tools and applications, Edited by R.S. Soin, F. Maloberti and J. Franca, IEE Publications 2. Signal Integrity Effects in Custom IC and ASIC Designs, Raminderpal Singh (Editor), Wiley Publications	**References-** 1. 1. Analogue-digital ASICs: circuit techniques, design tools and applications, Edited by R.S. Soin, F. Maloberti and J. Franca, IEE Publications 2. Signal Integrity Effects in Custom IC and ASIC Designs, Raminderpal Singh (Editor), Wiley Publications

6. Elective – II E15 (E)AUTOMOTIVE EMBEDDED SYSTEMS	**AUTOMOTIVE EMBEDDED SYSTEMS**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Current trends in Automobiles, open loop and closed loop systems - components for electronic engine management system. Electromagnetic interference suppression. Electromagnetic compatibility, Electronic dashboard instruments, onboard diagnostic system ,	**Unit 1** **6 HRS** Current trends in Automobiles, open loop and closed loop systems - components for electronic engine management system. Electromagnetic interference suppression. Electromagnetic compatibility, Electronic dashboard instruments, onboard diagnostic system ,
Unit 2 **7 HRS** security and warmingsystem. Electronic management of chassis systems.Vehicle motion control.Sensors and actuators,and their interfacing. Basic sensor arrangement, types of sensors such as-oxygen sensors, crankangle position sensors- Fuel metering/ vehicle speed sensors and destination sensors, Attitude sensor,Flow sensor, exhaust temperature, air mass flow sensors. Throttle position sensor	**Unit 2** **7 HRS** security and warmingsystem. Electronic management of chassis systems.Vehicle motion control.Sensors and actuators,and their interfacing. Basic sensor arrangement, types of sensors such as-oxygen sensors, crankangle position sensors- Fuel metering/ vehicle speed sensors and destination sensors, Attitude sensor,Flow sensor, exhaust temperature, air mass flow sensors. Throttle position sensor
Unit 3 **6 HRS** solenoids, steppermotors, relays. Electronic ignition systems.Types of solid state ignition systems and their principleof operation.	**Unit 3** **6 HRS** solenoids, steppermotors, relays. Electronic ignition systems.Types of solid state ignition systems and their principleof operation.
Unit 4 **7 HRS**	**Unit 4** **7 HRS**

Digital engine control system. Open loop and closed loop control system, Enginecranking and warm up control. Acceleration enrichment. Deceleration learning and ideal speedcontrol, Distributor less ignition – Integrated engine control system, Exhaust emission controlengineering.	Digital engine control system. Open loop and closed loop control system, Enginecranking and warm up control. Acceleration enrichment. Deceleration learning and ideal speedcontrol, Distributor less ignition – Integrated engine control system, Exhaust emission controlengineering.
Unit 5 **6 HRS** Automotive Embedded systems. PIC, Freescale microcontroller based system. Recentadvances like GLS, GPSS, GMS. Multiprocessor communication using CAN bus.	**Unit 5** **6 HRS** Automotive Embedded systems. PIC, Freescale microcontroller based system. Recentadvances like GLS, GPSS, GMS. Multiprocessor communication using CAN bus.
Unit 6 **7 HRS** Case study- cruisecontrol of car. Artificial Intelligence and engine management	**Unit 6** **7 HRS** Case study- cruisecontrol of car. Artificial Intelligence and engine management
References: 1. William B. Riddens, “Understanding Automotive Electronics”, 5th Edition, Butterworth Hennimann Woburn, 1998. 2. Young A.P. & Griffiths, “ Automotive Electrical Equipment” , ELBS & New Press-1999 3. Tom Weather Jr. &Cland c. Ilunter, “ Automotive computers and control system”Prentice Hall Inc., New Jersey. 4. Crouse W.H., “ Automobile Electrical Equipment” , McGraw Hill Co. Inc., New York ,1995. 5. Bechhold, “ Understanding Automotive Electronic”, SAE,1998. 6. Robert Bosch,” Automotive Hand Book”, SAE (5TH Edition),2000.	**References:** 1. William B. Riddens, “Understanding Automotive Electronics”, 5th Edition, Butterworth Hennimann Woburn, 1998. 2. Young A.P. & Griffiths, “ Automotive Electrical Equipment” , ELBS & New Press-1999 3. Tom Weather Jr. &Cland c. Ilunter, “ Automotive computers and control system”Prentice Hall Inc., New Jersey. 4. Crouse W.H., “ Automobile Electrical Equipment” , McGraw Hill Co. Inc., New York ,1995. 5. Bechhold, “ Understanding Automotive Electronic”, SAE,1998. 6. Robert Bosch,” Automotive Hand Book”, SAE (5TH Edition),2000.

R123

7. S 16 Seminar-I	Seminar-I
Old Syllabus	**New Syllabus**
Teaching Scheme : P : 2 hrs/ Week/student Credits: 2	Teaching Scheme : P : 2 hrs/ Week/student Credits: 2
Students shall deliver Seminar on the State-of-the-Art topic in front of Examiners and Student-colleagues. Prior to presentation, he/she shall carry out the detailed literature survey from Standard References such as International Journals and Periodicals, recently published reference Books etc. and submit a report on the same along with computer based presentation copy to the concerned examiner/guide at the end of the seminar. The assessment shall be based on selection of topic, its relevance to the present context, report documentation and presentation skills. Guide should spare(Guide) for 2hrs /week/student for seminar	The topic of seminar shall be based on area of Environmental Engineering & preferably considering new ideas, concepts, technologies & developments in the field of Environmental Sciences & Technologies. At least two oral presentations and submission of report in soft & hard copies is expected. Students shall deliver Seminar on the State-of-the-Art topic in front of Examiners and Student-colleagues. Prior to presentation, he/she shall carry out the detailed literature survey from Standard References such as International Journals and Periodicals, recently published reference Books etc. and submit a report on the same along with computer based presentation copy to the concerned examiner/guide at the end of the seminar. The assessment shall be based on selection of topic, its relevance to the present context, report documentation and presentation skills. Guide should spare for 2hrs /week/student for seminar

8. C 14 High Speed Analog Design Lab	High Speed Analog Design Lab
Old Syllabus	**New Syllabus**
Teaching Scheme : P : 2 hrs/week Credits: 1	Teaching Scheme : P : 2 hrs/week Credits: 1
Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.	Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.

9. C 15 Reconfigurable Platforms & HDL Lab	**Reconfigurable Platforms & HDL Lab**
Teaching Scheme : P : 2 hrs/week Credits: 1	Teaching Scheme : P : 2 hrs/week Credits: 1
Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.	Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.
10. C 16 Communication Network Lab	**Communication Network Lab**
Teaching Scheme : P : 2 hrs/week Credits: 1	Teaching Scheme : P : 2 hrs/week Credits: 1
Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.	Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.

Shivaji University, Kolhapur First Year M. Tech Electronics Technology (Semester II)	
1. C 21 DSP Processors	**DSP Processors**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 4hrs/week Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 4hrs/week Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Introduction to TMS320C6x processor, architecture, pipelining, linear and circular addressing modes, TMS320C6x instruction set, assembler directives, timers, interrupts, serial I/O, DMA, fixed and floating point data format,	**Unit 1** **6 HRS** Introduction to various architectures of TMS320C6x processor, architecture, pipelining, linear and circular addressing modes, TMS320C6x instruction set, assembler directives, timers, interrupts, serial I/O, DMA, fixed and floating point data format,
Unit 2 **7 HRS** Digital signal processing and DSP systems: Advantages of DSP, characteristics of DSP systems, DSP applications. DSP processors, architecture and instruction set.	**Unit 2** **7 HRS** Digital signal processing and DSP systems: Advantages of DSP, characteristics of DSP systems, DSP applications. DSP processors.
Unit 3 **6 HRS** Numeric representations and arithmetic: floating point numbers, IEEE 754 standard for floating point numbers,	**Unit 3** **6 HRS** Numeric representations and arithmetic: floating point numbers, architecture and instruction set
Unit 4 **7 HRS** Memory Architectures: memory structures, wait states, extended memory interfaces, addressing mechanisms.	**Unit 4** **7 HRS** Memory Architectures: memory structures wait states, extended memory interfaces, addressing mechanisms.
Unit 5 **6 HRS** Execution control: Hardware looping, interrupts, stack, relative branch support Pipelining: pipelining and performance, pipelining depth, interlocking, branching effects, interrupt effects,	**Unit 5** **6 HRS** Execution control: Hardware looping, interrupts, stack, relative branch support Pipelining: pipelining and performance, pipelining depth, interlocking, branching effects, interrupt effects,
Unit 6 **6 HRS** Peripherals: serial / parallel ports, timers, communication ports, on-chip A^D and D/A converters,-external interrupts, on-chip debugging facilities, power consumption, clocking.	**Unit 6** **6 HRS** Peripherals: serial / parallel ports, timers, communication ports, on-chip A^D and D/A converters,-external interrupts, on-chip debugging facilities, power consumption, clocking.
Books: 1. DSP Processor Fundamentals: architectures and Features, by Phil Lapsley, Wiley 2. DSP Applications using C and the TMS320C6x DSP	**Books:** 1. DSP Processor Fundamentals: architectures and Features, by Phil Lapsley, Wiley 2. DSP Applications using C and the TMS320C6x DSP

2.C22 REAL TIME OPERATING SYSTEMS	REAL TIME OPERATING SYSTEMS
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3hrs/week T:-- Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3hrs/week T:1 Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++	**Unit 1** **6 HRS** Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++
Unit 2 **7 HRS** Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance, Operating System Concepts	**Unit 2** **7 HRS** Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance, Operating System Concepts
Unit 3 **6 HRS** Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts. Operating system structure Monolithic Systems: Layered Systems,Virtual Machines, Exo-kernels, Client-Server Model	**Unit 3** **6 HRS** Processes, Deadlocks, Memory Management, Input /Output, Files, Security, the Shell, Recycling of Concepts. Operating system structure Monolithic Systems: Layered Systems,Virtual Machines, Exo-kernels, Client-Server Model
Unit 4 **7 HRS** Real Time Operating Systems (µC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting µCos-II. REAL TIME KERNEL Principles – Design issues – Polled Loop Systems –RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.	**Unit 4** **7 HRS** Real Time Operating Systems (µC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting µCos-II. REAL TIME KERNEL Principles – Design issues – Polled Loop Systems –RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.
Unit 5 **6 HRS** Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management.	**Unit 5** **6 HRS** Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management.
Unit 6 **7 HRS** RTOS APPLICATION DOMAINS vizRTOS for Image Processing – Embedded RTOS for voice	**Unit 6** **7 HRS** RTOS APPLICATION DOMAINS vizRTOS for Image Processing – Embedded RTOS for voice

over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.	over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.
References: 1. µC/OS-II, The real time Kernel, Jean J. Labrossy, Lawrence: R & D Publications. 2. Embedded Real Time Systems: Concepts, Design & Programming, Dr.K.V.K.K. Prasad, Dreamtech Publication. 3. An Embedded Software Primer, David E. Simon, Pearson Education Publication. 4. Modern Operating Systems, Second Edition, Andrew S. Tanenbaum, Prentice Hall Publication.	**References:** 1. µC/OS-II, The real time Kernel, Jean J. Labrossy, Lawrence: R & D Publications. 2. Embedded Real Time Systems: Concepts, Design & Programming, Dr.K.V.K.K. Prasad, Dreamtech Publication. 3. An Embedded Software Primer, David E. Simon, Pearson Education Publication. 4. Modern Operating Systems, Second Edition, Andrew S. Tanenbaum, Prentice Hall Publication.

3. C23 Mobile Computing	**Mobile Computing**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** 1G to 4G mobile telephone technologies.	**Unit 1** **6 HRS** Cellular Communication Fundamentals: Cellular system design, Frequency reuse, cell splitting, handover concepts, Co channel and adjacent channel interference, interference reduction techniques and methods to improve cell coverage, Frequency management and channel assignment.GSM architecture and interfaces, GSM architecture details, GSM subsystems, GSM Logical Channels, Data Encryption in GSM, Mobility Management, Call Flows in GSM. Multiple access technologies: Comparison of TDMA, FDMA and CDMA technologies based on their signal separation techniques, advantages, disadvantages and application areas, spectral efficiency calculations for these techniques.
Unit 2 **7 HRS** Reference architectures for wireless LAN, WLANGPRS.	**Unit 2** **7 HRS** Code Division Multiple Access: Introduction to CDMA technology, IS 95 system Architecture, Air Interface, Physical and logical channels of IS 95, Forward Link and Reverse link operation, Physical and Logical channels of IS 95 CDMA, IS 95 CDMA Call Processing, soft Handoff Evolution of IS 95 (cdmaOne) to cdma 2000, cdma 2000 layering

	structure and channels. Higher Generation Cellular Standards: 2.5 G Standards: High speed Circuit Switched Data (HSCSD), General Packet Radio Service (GPRS), 2.75 G Standards: EDGE, 3 G Standards: evolved EDGE, enhancements in 4G standard.
Unit 3 **7 HRS** GSM and VOIP architecture, 4-G LTE network architecture and protocols	**Unit 3** **7 HRS** Reference architectures for wireless LAN.
Unit 4 **6 HRS** Transmitdiversity and MIMO spatial multiplexing,	**Unit 4** **6 HRS** OFDM: Introduction to OFDM, Multicarrier Modulation and cyclic prefix, Channel model and SNR performance, OFDM issues –PAPR, Frequency and timing offset issues.
Unit 5 **7 HRS** Applications of Mobile computing Business valuebehind mobile application development Best practices for the entire project life cycle.	**Unit 5** **7 HRS** MIMO: Introduction to MIMO, MIMO channel capacity, SVG and Eigen modes of the MIMO channel, MIMO spatial multiplexing— BLAST, MIMO diversity – Alamouti, OSTBC, MRT, MIMO – OFDM.
Unit 6 **6 HRS** Casestudies secure mobile application development Fundamentals of wireless Mark up language WML script applications.	**Unit 6** **6 HRS** UWB (Ultrawide Band): UWB definations and features, UWB wireless channels, UWB data modulation, Uniform pulse train, Bit Error Rate performance of UWB.
References- 1. Introduction to Mobile Telephone Systems, 2nd Edition, 1G, 2G, 2.5G, and 3G Technologies and Services by Lawrence Harte 2. Wireless and Mobile Data Networks by Aftab Ahmad 3. Wireless and Mobile Network Architectures by Yi-Bing Lin and ImrichChlamtac 4. Mobile Applications: Architecture, Design, and Development by Valentino Lee, Heather Schneider, and Robbie Schell 5. Mobile IP Technology and Applications by Stefan Raab and Madhavi W. Chandra 6. Mobile Application Security [Paperback] HimanshuDwivedi (Author), Chris Clark , David Thiel. 7. Beginning WAP: Wireless Markup Language & Wireless Markup	**References-** 1. Introduction to Mobile Telephone Systems, 2nd Edition, 1G, 2G, 2.5G, and 3G Technologies and Services by Lawrence Harte 2. Wireless and Mobile Data Networks by Aftab Ahmad 3. Wireless and Mobile Network Architectures by Yi-Bing Lin and ImrichChlamtac 4. Mobile Applications: Architecture, Design, and Development by Valentino Lee, Heather Schneider, and Robbie Schell 5. Mobile IP Technology and Applications by Stefan Raab and Madhavi W. Chandra 6. Mobile Application Security [Paperback] HimanshuDwivedi (Author), Chris Clark , David Thiel. 7. Beginning WAP: Wireless Markup Language & Wireless Markup

Language Script by SooMee Foo, Ted Wugofski, Wei Meng Lee, and Foo SooMee 8.WML &WMLScript: A Beginner's Guide by Kris A. Jamsa	Language Script by SooMee Foo, Ted Wugofski, Wei Meng Lee, and Foo SooMee 8.WML &WMLScript: A Beginner's Guide by Kris A. Jamsa

4. E 24 (V) Systems on Chip	**Systems on Chip**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3hrs/week T: -- Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3hrs/week T: 1 Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** IC Technology, Economics, CMOS Technology overview, Power consumption, Hierarchical design, Design Abstraction, EDA tools.	**Unit 1** **6 HRS** IC Technology, Economics, CMOS Technology overview, Power consumption, Hierarchical design, Design Abstraction, EDA tools.
Unit 2 **7 HRS** MOSFET model, parasitics, latch up, advanced transistor structures; Wire parasitics; Design rules, Scalable design rules, process parameters; stick diagrams, Layout design tools; Layout synthesis, layout analysis.	**Unit 2** **7 HRS** MOSFET model, parasitics, latch up, advanced transistor structures; Wire parasitics; Design rules, Scalable design rules, process parameters; stick diagrams, Layout design tools; Layout synthesis, layout analysis.
Unit 3 **6 HRS** CMOS gate delays, transmission time, speed power product, low power gates; Delay by RC trees, cross talk, RLC delay, cell based layout, Logic & interconnect design, delay modeling, wire sizing; Power optimization, Switch logic networks.	**Unit 3** **6 HRS** CMOS gate delays, transmission time, speed power product, low power gates; Delay by RC trees, cross talk, RLC delay, cell based layout, Logic & interconnect design, delay modeling, wire sizing; Power optimization, Switch logic networks.
Unit 4 **7 HRS** Pipelining, Data paths, Adders, ALUs, Multipliers, High density memories; Metastability, Multiphase clocking; Power optimization, Design validation, Sequential testing; Architecture for low power.	**Unit 4** **7 HRS** Pipelining, Data paths, Adders, ALUs, Multipliers, High density memories; Metastability, Multiphase clocking; Power optimization, Design validation, Sequential testing; Architecture for low power.
Unit 5 **6 HRS** Floor planning methods, global routing, switch box routing, clock distribution; off chip connections, packages, I/O architectures, pad design.	**Unit 5** **6 HRS** Floor planning methods, global routing, switch box routing, clock distribution; off chip connections, packages, I/O architectures, pad design.
Unit 6 **7 HRS** Complete chip design including architecture, logic and layout for Kitchen timer chip OR Microwave oven chip	**Unit 6** **7 HRS** Complete chip design including architecture, logic and layout for Kitchen timer chip OR Microwave oven chip
Reference books: *1. Wayne Wolf, "Modern VLSI Design", Pearson Education.* 2. *KamaranEshraghian, "Principles of CMOS VLSI Design", Pearson*	*Reference books:* *1. Wayne Wolf, "Modern VLSI Design", Pearson Education.* 2. *KamaranEshraghian, "Principles of CMOS VLSI Design", Pearson*

Education 3. *Rabey, Chandrakasan, "Digital IC Design", Pearson Publication*	*Education* 3. *Rabey, Chandrakasan, "Digital IC Design", Pearson Publication*

4. E 24 (V) Wavelet Transform and its applications	**Wavelet Transform and its applications**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Introduction, Continuos-Time Wavelets, Definition of the CWT, The CWT as a Correlation. Constant Q -Factor Filteing Interpretation and Time-Frequency resolution, The CWT as an Operator, Inverse CWT.	**Unit 1** **6 HRS** Introduction, Continuos-Time Wavelets, Definition of the CWT, The CWT as a Correlation. Constant Q -Factor Filteing Interpretation and Time-Frequency resolution, The CWT as an Operator, Inverse CWT.
Unit 2 **7 HRS** Introduction, Approximation of Vectors in Nested Linear Vector Subspaces, **(i)**Example of Approximating Vectors in Nested Subspaces of a Finite-Dimensional Linear Vectors Space, **(ii)** Example of Approximating Vectors in Nested Subspaces of an infinite- Dimensional Linear Vectors space, Example of an MRA, **(i)** Bases for the Approximation subspaces and Haar Scaling function, **(ii)** Bases for the Detail Subspaces and Haar Wavelet, **(iii)** Digital Filter Implementation of the Haar Wavelet Decomposition.	**Unit 2** **7 HRS** Introduction, Approximation of Vectors in Nested Linear Vector Subspaces, **(i)**Example of Approximating Vectors in Nested Subspaces of a Finite-Dimensional Linear Vectors Space, **(ii)** Example of Approximating Vectors in Nested Subspaces of an infinite- Dimensional Linear Vectors space, Example of an MRA, **(i)** Bases for the Approximation subspaces and Haar Scaling function, **(ii)** Bases for the Detail Subspaces and Haar Wavelet, **(iii)** Digital Filter Implementation of the Haar Wavelet Decomposition.
Unit 3 **6 HRS** Introduction, Formal Definition of an MRA, Construction of a General Orthonormal MRA, **(i)** Scaling Function and Subspaces, **(ii)** Implication of the Dilation Equation and Ortliogonality, A wavelet Basis for the MRA **(i)** Two scale Relation for (t), **(ii)** Basis for the detail subspaces **(iii)** Direct sum decomposition, Digital Filtering interpretation. **(i)** Decomposition Filters, **(ii)** Reconstructing the Signal. Examples of Orthogonal Basis-Generating Wavelets, **(i)** Daubechies D4 Scaling Function and Wavelet, **(ii)** Band limited Wavelets, Interpreting Orthonormal MRAs for 40	**Unit 3** **6 HRS** Introduction, Formal Definition of an MRA, Construction of a General Orthonormal MRA, **(i)** Scaling Function and Subspaces, **(ii)** Implication of the Dilation Equation and Ortliogonality, A wavelet Basis for the MRA **(i)** Two scale Relation for (t), **(ii)** Basis for the detail subspaces **(iii)** Direct sum decomposition, Digital Filtering interpretation. **(i)** Decomposition Filters, **(ii)** Reconstructing the Signal. Examples of Orthogonal Basis-Generating Wavelets, **(i)** Daubechies D4 Scaling Function and Wavelet, **(ii)** Band limited Wavelets, Interpreting Orthonormal MRAs for 40

Discrete-Time Signals, **(i)** Continuous-Time MRA interpretation for DTWT, **(ii)** Discrete-Time MRA, **(iii)** Basis Functions for the DTWT, Miscellaneous issues related to PRQMF Filter Banks, Generating Scaling Functions and Wavelets from Filter Coefficients	Discrete-Time Signals, **(i)** Continuous-Time MRA interpretation for DTWT, **(ii)** Discrete-Time MRA, **(iii)** Basis Functions for the DTWT, Miscellaneous issues related to PRQMF Filter Banks, Generating Scaling Functions and Wavelets from Filter Coefficients
Unit 4 **7 HRS** Introduction, Biorthogonal Wavelet Bases, Filtering Relationship for Biorthogonal Filters, Examples of Biorthogonal Scaling Functions and Wavelets, Two-Dimensional Wavelets, Nonseparable Multidimensional Wavelets, Wavelet packets.	**Unit 4** **7 HRS** Introduction, Biorthogonal Wavelet Bases, Filtering Relationship for Biorthogonal Filters, Examples of Biorthogonal Scaling Functions and Wavelets, Two-Dimensional Wavelets, Nonseparable Multidimensional Wavelets, Wavelet packets.
Unit 5 **6 HRS** Introduction, Transform coding, DTWT for Image Compression, **(i)** Image Compression using DTWT and Run-Length Encoding, **(ii)** Embedded Tree Image Coding, **(iii)** Comparison with JPEG, Audio Compression. **(I)** Audio Masking, **(ii)** Standards Specifying Subband Implementation: ISO/MPEG Coding for Audio, **(iii)** Wavelet-Based Audio Coding, Video Coding Using Multiresolution Techniques: A Brief Introduction.	**Unit 5** **6 HRS** Introduction, Transform coding, DTWT for Image Compression, **(i)** Image Compression using DTWT and Run-Length Encoding, **(ii)** Embedded Tree Image Coding, **(iii)** Comparison with JPEG, Audio Compression. **(I)** Audio Masking, **(ii)** Standards Specifying Subband Implementation: ISO/MPEG Coding for Audio, **(iii)** Wavelet-Based Audio Coding, Video Coding Using Multiresolution Techniques: A Brief Introduction.
Unit 6 **7 HRS** Introduction, Wavelet Denoising, Speckle Removal, Edge Detection and Object Isolation, Image Fusion, Object Detection by Wavelet Transforms of Projrctions, Communication Applications, **(i)** Scaling Functions as Signaling Pulses, **(ii)** Discrete Wavelet Multitone Modulation	**Unit 6** **7 HRS** Introduction, Wavelet Denoising, Speckle Removal, Edge Detection and Object Isolation, Image Fusion, Object Detection by Wavelet Transforms of Projrctions, Communication Applications, **(i)** Scaling Functions as Signaling Pulses, **(ii)** Discrete Wavelet Multitone Modulation
Text Book: **1.** Wavelet Transforms - Introduction to Theory & Applications, RaguhuveerM.Rao&Ajit S. Bopadikar - Addison Wesley-1998 **Reference Book:** **1.** Wavelets and Filter Banks, Gilbert Stang& Truong Nguyen-	**Text Book:** **1.** Wavelet Transforms - Introduction to Theory & Applications, RaguhuveerM.Rao&Ajit S. Bopadikar - Addison Wesley-1998 **Reference Book:** **1.** Wavelets and Filter Banks, Gilbert Stang& Truong Nguyen-

Wellesly -1996 References : 1.P. P. Vaidyanathan: Multirate Systems & Filter Banks, PTR, PH, 19932.Gilbert Strang : Linear Algebra and its Applications.3.Reghuveer M Rao, Ajit S Bopardikar: Wavelet Transforms 2.Introduction to Theory and Applications, Pearson Education Asia, 1998.4.Strang G S, T Q Nguyen:Wavelets and Filter Banks, 3. WellesleyCambridge Press 1996.5.Burrus C S, R A Gopinath and H. Gao: Introduction to Wavelets and Wavelet Transforms: APrimer , Prentice Hall, 1998.	Wellesly -1996 References : 1.P. P. Vaidyanathan: Multirate Systems & Filter Banks, PTR, PH, 19932.Gilbert Strang : Linear Algebra and its Applications.3.Reghuveer M Rao, Ajit S Bopardikar: Wavelet Transforms 2.Introduction to Theory and Applications, Pearson Education Asia, 1998.4.Strang G S, T Q Nguyen:Wavelets and Filter Banks, 3. WellesleyCambridge Press 1996.5.Burrus C S, R A Gopinath and H. Gao: Introduction to Wavelets and Wavelet Transforms: APrimer , Prentice Hall, 1998.

4. E 24 (E) Microelectromechanical Systems	**Microelectromechanical Systems**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** History of MicroElectroMechanical Systems (MEMS), market for MEMS, basics of microtechnology, lithography and etching techniques,	**Unit 1** **6 HRS** History of MicroElectroMechanical Systems (MEMS), market for MEMS, basics of microtechnology, lithography and etching techniques,
Unit 2 **7 HRS** principles of bulk and surface micromachining: subtractive processes, additive processes (evaporation, sputtering, epitaxial growth). Fundamental devices and processes, Multi User MEMS Process (MUMPs), SUMMiT: design rules; applications; micro hinges and deployment actuators,	**Unit 2** **7 HRS** principles of bulk and surface micromachining: subtractive processes, additive processes (evaporation, sputtering, epitaxial growth). Fundamental devices and processes, Multi User MEMS Process (MUMPs), SUMMiT: design rules; applications; micro hinges and deployment actuators,
Unit 3 **6 HRS** CMOS MEMS, cleanroom lab techniques, MicroOptoElectroMechanical Systems (MOEMS), bioMEMS and biomaterials, piezoresistivity; scanning probe microscopy, scaling laws, applications.	**Unit 3** **6 HRS** CMOS MEMS, cleanroom lab techniques, MicroOptoElectroMechanical Systems (MOEMS), bioMEMS and biomaterials, piezoresistivity; scanning probe microscopy, scaling laws, applications.
Unit 4 **7 HRS** Lumped element modeling and design, Electrostatic Actuators , Electromagnetic Actuators, Linear and nonlinear system dynamics, resonant systems, Elasticity (stress, strain, material	**Unit 4** **7 HRS** Lumped element modeling and design, Electrostatic Actuators , Electromagnetic Actuators, Linear and nonlinear system dynamics, resonant systems, Elasticity (stress, strain, material properties),

properties), Mechanical structure basics (bending of bes, torsion,natural frequency), Optical system design basics (Gaussian beam optics, matrix optics, resolution)	Mechanical structure basics (bending of bes, torsion,natural frequency), Optical system design basics (Gaussian beam optics, matrix optics, resolution)
Unit 5 **6 HRS** Application case studies: MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micromirror Devices (DMD),	**Unit 5** **6 HRS** Application case studies: MEMS Scanners and Retinal Scanning Displays (RSD), Grating Light Valve (GLV), Digital Micromirror Devices (DMD),
Unit 6 **7 HRS** Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT)	**Unit 6** **7 HRS** Optical switching, Capacitive Micromachined Ultrasonic Transducers (CMUT)
Reference Books: 1. Gregory T A 1998, Kovacs Micromachined Transducers Sourcebook, WCB McGraw-Hill. 2. NadimMaluf, An introduction to Microelectromechanical system design, Artech House, 2000 3. Victor M. Bright, Editor, Selected papers on Optical MEMS, SPIE Milestone Series, Volume MS 153, SPIE Press, 1999 4. Mohamed Gad-el-Hak, Editor, The MEMS Handbook, CRC Press, Baco Raton, 2001 5. Marc Madou, Fundamentals of Microfabrication, CRC Press, New York, 1997. 6. Gregory T. A. Kovacs, Micromachined Transducers Sourcebook, WCB / McGraw-Hill 7. W. Trimmer, Editor, Micromechanics and MEMS: Classic and Seminal Papers to 1990, IEEE Press 1	**Reference Books:** 1. Gregory T A 1998, Kovacs Micromachined Transducers Sourcebook, WCB McGraw-Hill. 2. NadimMaluf, An introduction to Microelectromechanical system design, Artech House, 2000 3. Victor M. Bright, Editor, Selected papers on Optical MEMS, SPIE Milestone Series, Volume MS 153, SPIE Press, 1999 4. Mohamed Gad-el-Hak, Editor, The MEMS Handbook, CRC Press, Baco Raton, 2001 5. Marc Madou, Fundamentals of Microfabrication, CRC Press, New York, 1997. 6. Gregory T. A. Kovacs, Micromachined Transducers Sourcebook, WCB / McGraw-Hill 7. W. Trimmer, Editor, Micromechanics and MEMS: Classic and Seminal Papers to 1990, IEEE Press 1

4. E 24 (E) Robotics and Machine Vision	**Robotics and Machine Vision**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Robotics – Introduction–Basic Structure– Classification of robot and Robotic systems –laws of	**Unit 1** **6 HRS** Robotics – Introduction–Basic Structure– Classification of robot and Robotic systems –laws of

robotics – robot motions – work space, precision of movement. Drives and control systems: Hydraulic systems, power supply – servo valve – sump – hydraulic motor – DC servo motors – stepper motors – operation. Mechanical Components of Robots: Power transmission systems: Gear transmission. Belt drives, cables, Roller Chains, Link – Road Systems, Rotary to linear motion conversion, Ract and pinion drives, ball bearing screws, speed reducers, Harmonic drives.	robotics – robot motions – work space, precision of movement. Drives and control systems: Hydraulic systems, power supply – servo valve – sump – hydraulic motor – DC servo motors – stepper motors – operation. Mechanical Components of Robots: Power transmission systems: Gear transmission. Belt drives, cables, Roller Chains, Link – Road Systems, Rotary to linear motion conversion, Ract and pinion drives, ball bearing screws, speed reducers, Harmonic drives.
Unit 2 **6 HRS** Kinematics of Robot: Introduction, Matrix Representation, Homogeneous transformation, forward and inverse Kinematics, Inverse Kinematics Programming, Degeneracy, dexterity, velocity and static forces, velocity transformation force control systems, Basics of Trajectory planning.	**Unit 2** **6 HRS** Kinematics of Robot: Introduction, Matrix Representation, Homogeneous transformation, forward and inverse Kinematics, Inverse Kinematics Programming, Degeneracy, dexterity, velocity and static forces, velocity transformation force control systems, Basics of Trajectory planning.
Unit 3 **7 HRS** Robot End Effectors: Types of end effectors – Mechanical grippers – Types of Gripper mechanisms – Grippers force analysis – Other types of Grippers – Vacuum cups – Magnetic Grippers – Adhesive Grippers – Robot end effector interface. Sensors: Position sensors – Potentiometers, encoders – LVDT, Velocity sensors, Acceleration Sensors, Force, Pressure and Torque sensors, Touch and Tactile sensors, Proximity, Range and sniff sensors, RCC, VOICE recognition and synthesizers.	**Unit 3** **7 HRS** Robot End Effectors: Types of end effectors – Mechanical grippers – Types of Gripper mechanisms – Grippers force analysis – Other types of Grippers – Vacuum cups – Magnetic Grippers – Adhesive Grippers – Robot end effector interface. Sensors: Position sensors – Potentiometers, encoders – LVDT, Velocity sensors, Acceleration Sensors, Force, Pressure and Torque sensors, Touch and Tactile sensors, Proximity, Range and sniff sensors, RCC, VOICE recognition and synthesizers.
Unit 4 **6 HRS** Machine Vision: Introduction – Image processing Vs image analysis, image Acquisition, digital Images – Sampling and Quantization – Image definition, levels of Computation.	**Unit 4** **6 HRS** Machine Vision: Introduction – Image processing Vs image analysis, image Acquisition, digital Images – Sampling and Quantization – Image definition, levels of Computation.
Unit 5 **7 HRS** Image processing Techniques: Data reduction – Windowing, digital conversion. Segmentation – Thresholding, Connectivity, Noise Reduction, Edge detection, Segmentation, Region growing and Region Splitting, Binary Morphology and grey morphology operations	**Unit 5** **7 HRS** Image processing Techniques: Data reduction – Windowing, digital conversion. Segmentation – Thresholding, Connectivity, Noise Reduction, Edge detection, Segmentation, Region growing and Region Splitting, Binary Morphology and grey morphology operations
Unit 6 **7 HRS** Feature Extraction: Geometry of curves – Curve approximation, Texture and texture analysis, Image resolution – Depth and volume, Color processing, Object recognition by features, Depth measurement, specialized lighting techniques. Segmentation using motion – Tracking. Image Data Compression, Real time Image	**Unit 6** **7 HRS** Feature Extraction: Geometry of curves – Curve approximation, Texture and texture analysis, Image resolution – Depth and volume, Color processing, Object recognition by features, Depth measurement, specialized lighting techniques. Segmentation using motion – Tracking. Image Data Compression, Real time Image

processing, Application of Vision systems.	processing, Application of Vision systems.
TEXT BOOK 1.Saeed B. Niku, Introduction to Robotics: Analysis, Systems, Applications, 2nd edition, Pearson Education India, PHI 2003 (ISBN 81-7808-677-8) REFERENCES 1. M.P. Groover, Industrial Robotics – Technology, Programming and Applications, McGraw-Hill, USA, 1986. 2. Ramesh Jam, RangachariKasturi, Brain G. Schunck, Machine Vision, Tata McGraw-Hill, 1991. 3. Yoremkoren, Robotics for Engineers, McGraw-Hill, USA, 1987. 4. P.A. Janaki Raman, Robotics and Image Processing, Tata McGraw-Hill, 1991.	TEXT BOOK 1.Saeed B. Niku, Introduction to Robotics: Analysis, Systems, Applications, 2nd edition, Pearson Education India, PHI 2003 (ISBN 81-7808-677-8) REFERENCES 1. M.P. Groover, Industrial Robotics – Technology, Programming and Applications, McGraw-Hill, USA, 1986. 2. Ramesh Jam, RangachariKasturi, Brain G. Schunck, Machine Vision, Tata McGraw-Hill, 1991. 3. Yoremkoren, Robotics for Engineers, McGraw-Hill, USA, 1987. 4. P.A. Janaki Raman, Robotics and Image Processing, Tata McGraw-Hill, 1991.

5. E25(V) RF Integrated Circuit Design	**RF Integrated Circuit Design**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Introduction to MOSFET Devices, MOSFET modeling, Spice model, Device parasitics, RF modeling, Parasitics sensitive to RF.	**Unit 1** **6 HRS** Introduction to MOSFET Devices, MOSFET modeling, Spice model, Device parasitics, RF modeling, Parasitics sensitive to RF.
Unit 2 **6 HRS** Issue in RF IC a brief review, Impedance matching, use anddesign of passive circuits, LNA Design.	**Unit 2** **6 HRS** Issue in RF IC a brief review, Impedance matching, use anddesign of passive circuits, LNA Design.
Unit 3 **7 HRS** Matching Techniques using algebra techniques, Basic Bondcircuits, UHF Mixer design.	**Unit 3** **7 HRS** Matching Techniques using algebra techniques, Basic Bondcircuits, UHF Mixer design.
Unit 4 **6 HRS** Cross talk, Cross connect architecture, Cross Connect characteristics,classification, Cross connect mechanism, Cross connect mitigation, Cross connect reduction, multiple Cross connect sources.	**Unit 4** **6 HRS** Cross talk, Cross connect architecture, Cross Connect characteristics,classification, Cross connect mechanism, Cross connect mitigation, Cross connect reduction, multiple Cross connect sources.
Unit 5 **7 HRS** EMI, EMC, Importance in ASIC Design, Introduction, EDA Tool inASIC Design	**Unit 5** **7 HRS** EMI, EMC, Importance in ASIC Design, Introduction, EDA Tool inASIC Design
Unit 6 **6 HRS** Design Flow, testing, Environment, sources of EMI/RFI, Solutions.	**Unit 6** **6 HRS** Design Flow, testing, Environment, sources of EMI/RFI, Solutions.
References-	**References-**

1. Thomas Lee, " RF IC Design" Oxford Press.. 2. T. Yettrdal, Yunhg Cheng, "Devices modeling for analog and RF COMS circuitsdesigne",John Wiley publication 2003. 1. Calvin Plett, "Radio frequency Integrated Circuits Design", Artech house.	1. Thomas Lee, " RF IC Design" Oxford Press.. 2. T. Yettrdal, Yunhg Cheng, "Devices modeling for analog and RF COMS circuitsdesigne",John Wiley publication 2003. 1. Calvin Plett, "Radio frequency Integrated Circuits Design", Artech house.

E 25 (E) High Performance Networks	**High Performance Networks**
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 3 hrs/week Credits: 3 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Types of Networks, Network design issues, Data in support of network design. Network design tools, protocols and architecture.	**Unit 1** **6 HRS** Types of Networks, Network design issues, Data in support of network design. Network design tools, protocols and architecture.
Unit 2 **7 HRS** VoIP system architecture,protocol hierarchy, Structure of a voice endpoint, Protocols for the transport ofvoice media over IP networks. Providing IP quality of service for voice, signaling protocols for VoIP, PSTN gateways, VoIP applications.	**Unit 2** **7 HRS** VoIP system architecture,protocol hierarchy, Structure of a voice endpoint, Protocols for the transport ofvoice media over IP networks. Providing IP quality of service for voice, signaling protocols for VoIP, PSTN gateways, VoIP applications.
Unit 3 **6 HRS** Introduction, challenges,SCSI protocols and architecture: RAID, Backup and mirroring, Fiber channelattached storage. Network attached storage including NFS, CIFS and DAFS,Management of network storage architectures.New storage protocols,architectures and enabling technologies.	**Unit 3** **6 HRS** Introduction, challenges,SCSI protocols and architecture: RAID, Backup and mirroring, Fiber channelattached storage. Network attached storage including NFS, CIFS and DAFS,Management of network storage architectures.New storage protocols,architectures and enabling technologies.
Unit 4 **7 HRS** Introduction to CDMA and spreadspectrum system, CDMA standards, system architectures of wirelesscommunication systems, physical, network and data link layer of CDMA, wireless LAN standards: IEEE 802.11b, ARPA.	**Unit 4** **7 HRS** Introduction to CDMA and spreadspectrum system, CDMA standards, system architectures of wirelesscommunication systems, physical, network and data link layer of CDMA, wireless LAN standards: IEEE 802.11b, ARPA.
Unit 5 **6 HRS** Overview of Information Theory. LosslessCompression: Run-Length Encoding, Facsimile compression, String-matchingAlgorithms.Lossy Compression: DCT, Wavelet compression.	**Unit 5** **6 HRS** Overview of Information Theory. LosslessCompression: Run-Length Encoding, Facsimile compression, String-matchingAlgorithms.Lossy Compression: DCT, Wavelet compression.
Unit 6 **7 HRS** A model for internet security, security attacks, services, internet	**Unit 6** **7 HRS** A model for internet security, security attacks, services, internet

standards &RFCs, Cryptography, Conventional encryption, principles and algorithms, cipherblock,modes of operation, location of encryption devices , key distribution,Public key cryptography principles and algorithms, RSA algorithm.	standards &RFCs, Cryptography, Conventional encryption, principles and algorithms, cipherblock,modes of operation, location of encryption devices , key distribution,Public key cryptography principles and algorithms, RSA algorithm.
Reference Books : 1. Kershenbaum A., "Telecommunications Network Design Algorithms", Tata McGraw Hill. 2. Ramaswami R., Shivrajan K, "Optical Networks", Morgan Kaufmann. 3. Douskalis B., "IP Telephony: The Integration of Robust VoIP Services", Pearson Ed. Asia. 4. Warland J., Varaiya P., "High-Performance Communication Networks", Morgan Kaufmann, 1996. 5. Stallings W., "High-Speed Networks: TCP/IP and ATM Design Principles", Prentice Hall,1998. 6. Garg V., Smolk K., VilkesJ.,"Applications of CDMA in wire less communication". 7. William Stalling : Network security, essentials- Pearson education Asia publication.	**Reference Books :** 1. Kershenbaum A., "Telecommunications Network Design Algorithms", Tata McGraw Hill. 2. Ramaswami R., Shivrajan K, "Optical Networks", Morgan Kaufmann. 3. Douskalis B., "IP Telephony: The Integration of Robust VoIP Services", Pearson Ed. Asia. 4. Warland J., Varaiya P., "High-Performance Communication Networks", Morgan Kaufmann, 1996. 5. Stallings W., "High-Speed Networks: TCP/IP and ATM Design Principles", Prentice Hall,1998. 6. Garg V., Smolk K., VilkesJ.,"Applications of CDMA in wire less communication". 7. William Stalling : Network security, essentials- Pearson education Asia publication.

E25 (E)High Speed Digital Design	
Old Syllabus	**New Syllabus**
Teaching Scheme : L : 4hrs/week Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40	Teaching Scheme : L : 4hrs/week Credits: 4 Evaluation Scheme: CIE SEE Minimum Passing Marks (25 + 25) 50 40
Unit 1 **6 HRS** Fundamental of high speed sampling, Base band antialiasing filters, Study of Harmonic sampling and band pass sampling, Direct IF to digital conversion, Distortion and noise in an ideal N bit ADC, AD9220 12 bit ADC, Spurious free Dynamic Range, Measurement of Noise Power Ratio, Flash converters, Case study of AD9066, Study of latency of ADCs,	**Unit 1** **6 HRS** Fundamental of high speed sampling, Base band antialiasing filters, Study of Harmonic sampling and band pass sampling, Direct IF to digital conversion, Distortion and noise in an ideal N bit ADC, AD9220 12 bit ADC, Spurious free Dynamic Range, Measurement of Noise Power Ratio, Flash converters, Case study of AD9066, Study of latency of ADCs,
Unit 2 **7 HRS** Driving ADC inputs for low distortion and wide dynamic range,	**Unit 2** **7 HRS** Driving ADC inputs for low distortion and wide dynamic range, Applications

Applications of high speed ADCs in CCD imaging, High speed ADC applications in Digital transceivers	of high speed ADCs in CCD imaging, High speed ADC applications in Digital transceivers
Unit 3 **6 HRS** Introduction to DDS, Aliasing in DDS Systems, 125 MSPS DDS System case study AD9850, DDS systems as ADC Clock Drivers.	**Unit 3** **6 HRS** Introduction to DDS, Aliasing in DDS Systems, 125 MSPS DDS System case study AD9850, DDS systems as ADC Clock Drivers.
Unit 4 **7 HRS** Amplitude modulation in a DDS System, The AD9831 Complete DDS System, High Speed low distortion DAC architecture, High Speed interpolating DACs, QPSK signal generation using DDS.	**Unit 4** **7 HRS** Amplitude modulation in a DDS System, The AD9831 Complete DDS System, High Speed low distortion DAC architecture, High Speed interpolating DACs, QPSK signal generation using DDS.
Unit 5 **6 HRS** Simulation tools, Prototyping Circuits, Grounding in high speed systems.	**Unit 5** **6 HRS** Simulation tools, Prototyping Circuits, Grounding in high speed systems.
Unit 6 **6 HRS** Power supply noise reduction and filtering, Power supply conditioning, EMI/RFI considerations, Shielding concepts	**Unit 6** **6 HRS** Power supply noise reduction and filtering, Power supply conditioning, EMI/RFI considerations, Shielding concepts
Reference Books: 1. High-Speed Digital Design: A Handbook of Black Magic by Howard Johnson 2. High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson 3. Signal Integrity Issues and Printed Circuit Board Design by Douglas Brooks 4. High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by Stephen H. Hall 5. Signal Integrity - Simplified by Eric Bogatin 6. Handbook of Digital Techniques for High-Speed Design : Design Examples, Signaling and Memory Technologies, Fiber Optics, Modeling, and Simulation to Ensure ... (Prentice Hall Modern Semiconductor Design) by Tom Granberg 7. Noise Reduction Techniques in Electronic Systems, 2nd Edition by Henry Ott 8. High Speed Design Techniques, Manual by analog Devices, October 1996	**Reference Books:** 1. High-Speed Digital Design: A Handbook of Black Magic by Howard Johnson 2. High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson 3. Signal Integrity Issues and Printed Circuit Board Design by Douglas Brooks 4. High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by Stephen H. Hall 5. Signal Integrity - Simplified by Eric Bogatin 6. Handbook of Digital Techniques for High-Speed Design : Design Examples, Signaling and Memory Technologies, Fiber Optics, Modeling, and Simulation to Ensure ... (Prentice Hall Modern Semiconductor Design) by Tom Granberg 7. Noise Reduction Techniques in Electronic Systems, 2nd Edition by Henry Ott 8. High Speed Design Techniques, Manual by analog Devices, October 1996

6. S26 Seminar-II	
Old Syllabus	**New Syllabus**
Teaching Scheme : P : 2 hrs/ Week/student Credits: 2	Teaching Scheme : P : 2 hrs/ Week/student Credits: 2
Students shall deliver Seminar on the State-of-the-Art topic in front of Examiners and Student-colleagues. Prior to presentation, he/she shall carry out the detailed literature survey from Standard References such as International Journals and Periodicals, recently published reference Books etc. and submit a report on the same along with computer based presentation copy to the concerned examiner/guide at the end of the seminar. The assessment shall be based on selection of topic, its relevance to the present context, report documentation and presentation skills. Guide should spare(Guide) for 2hrs /week/student for seminar	The topic of seminar shall be based on area of Environmental Engineering & preferably considering new ideas, concepts, technologies & developments in the field of Environmental Sciences & Technologies. At least two oral presentations and submission of report in soft & hard copies is expected. Students shall deliver Seminar on the State-of-the-Art topic in front of Examiners and Student-colleagues. Prior to presentation, he/she shall carry out the detailed literature survey from Standard References such as International Journals and Periodicals, recently published reference Books etc. and submit a report on the same along with computer based presentation copy to the concerned examiner/guide at the end of the seminar. The assessment shall be based on selection of topic, its relevance to the present context, report documentation and presentation skills. Guide should spare for 2hrs /week/student for seminar

7. C 24 DSP Processor Lab	
Old Syllabus	**New Syllabus**
Teaching Scheme : P : 2 hrs/week Credits: 1	Teaching Scheme : P : 2 hrs/week Credits: 1
Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.	Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.
8. C 25 Real Time Operating System Lab	
Teaching Scheme : P : 2 hrs/week Credits: 1	Teaching Scheme : P : 2 hrs/week Credits: 1

Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.	Students are instructed to frame and perform laboratory assignments, based on each of theory course. The assignment should encompass the hardware techniques and software tools introduced in the concerned subjects and should prove to be useful for the PG programs in the relevant discipline. Assignment should be a full-fledged system design type problem with multi-dimensional solutions suggested. Assignment should be implemented using known hardware techniques/software tools and should be reliably executable. Student shall submit a laboratory work document based on these assignments performed at the end of semester. The Laboratory instructor shall guide the students in framing the assignments and defining the problem pertaining to the said subjects.
9. C 26 Mobile computing	
Teaching Scheme : P : 2 hrs/week Credits: 1	Teaching Scheme : P : 2 hrs/week Credits: 1
- -	At the end of this course, students will demonstrate the ability to 1. Understanding Cellular concepts, GSM and CDMA networks. 2. To study GSM handset by experimentation and fault insertion techniques 3. Understating of 3G communication system by means of various AT commands usage in GSM 4. Understanding CDMA concept using DSSS kit 5. To learn, understand and develop concepts of Software Radio in real time environment

Shivaji University, Kolhapur Second Year M. Tech Electronics Technology (Semester III)		
Sr. No	**M. Tech (Electronics Technology) Semester III Pre-revised syllabus**	**M. Tech (Electronics Technology) Semester III Revised syllabus**
	Teaching Scheme : P : 2 hrs/week Credits: 4	Teaching Scheme : P : 2 hrs/week Credits: 4
1	Industrial Training	Industrial Training
	Industrial Training of 8 Weeks at the end of first year, evaluation at the end of third semester on the	Industrial Training of 8 Weeks at the end of first year OR

	basis of given report and presentation to concern guide.	Industrial Training will be split into two slots of Four weeks during semester III. Evaluation at the end of third semester on the basis of given report and presentation to concern guide.

Shivaji University, Kolhapur Second Year M. Tech Electronics Technology (Semester IV)		
Sr. No	**M. Tech (Electronics Technology)** **Semester III & IV** **Pre-revised syllabus**	**M. Tech (Electronics Technology)** **Semester IV** **Revised syllabus**
	Teaching Scheme : P : 5 hrs/week Credits: 20	Teaching Scheme : P : 5 hrs/week Credits: 20
1	Dissertation Phase – II	Dissertation Phase – II
	The student shall be allowed to submit the dissertation phase I report only after the completion of minimum 50% work of the total project with intermediate /partial results of the dissertation project to the concern guide and the dissertation phase II report only after the full-fledge demonstration of his /her work to the concerned guide. Assessment of the dissertation shall be based on design & implementation aspects, documentation & presentation skills, utility of the dissertation work & publications based on the same. For the dissertation phase I and phase II concern guide should guide to each student minimum for 2 hrs per week till the final submission of the dissertation of the concern student.	The student shall be allowed to submit the dissertation phase I report only after the completion of minimum 50% work of the total project with intermediate /partial results of the dissertation project to the concern guide and the dissertation phase II report only after the full-fledge demonstration of his /her work to the concerned guide. Assessment of the dissertation shall be based on design & implementation aspects, documentation & presentation skills, utility of the dissertation work & publications based on the same. For the dissertation phase I and phase II concern guide should guide to each student minimum for **2** hrs per week till the final submission of the dissertation of the concern student.